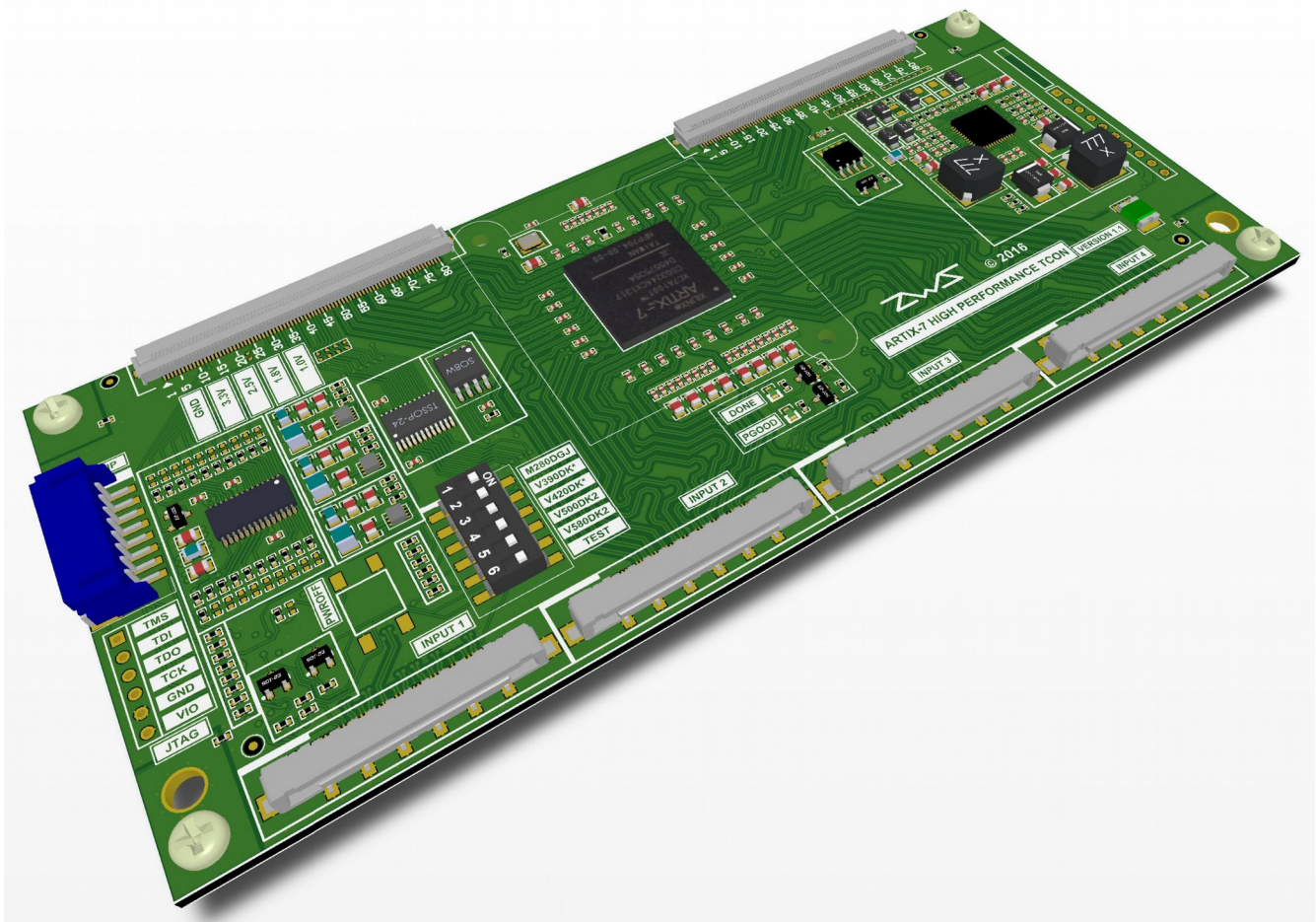


ZisWorks

“UHD TCON for Innolux Panels”

USER GUIDE



Document version : 18 August 2017

The latest version of this document and others can be found at:
zisworks.com/downloads

CHANGELOG

Version 1.0 : 19 July 2017 : Beta release (not posted online)

Version 1.1 : 18 August 2017 : Minor changes for public posting

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DISCLAIMER

The ZWS UHD TCON is a timing controller board for select models of UHD panels from the Innolux corporation. ZWS has no relationship with Innolux and has independently developed these products. Use of the ZWS TCON may violate some Innolux design specifications, and as such, will void any warranties of the panels.

OVERVIEW

The ZWS UHD TCON is an advanced timing controller board for select models of UHD panels from the Innolux corporation. With a high-performance Artix7 series FPGA from Xilinx, the ZWS UHD TCON offers system flexibility with some unique advantages over traditional TCONs. For the same panels. High refresh rate support, an integrated latency-free integer scaling, and

FEATURES AND SPECIFICATIONS

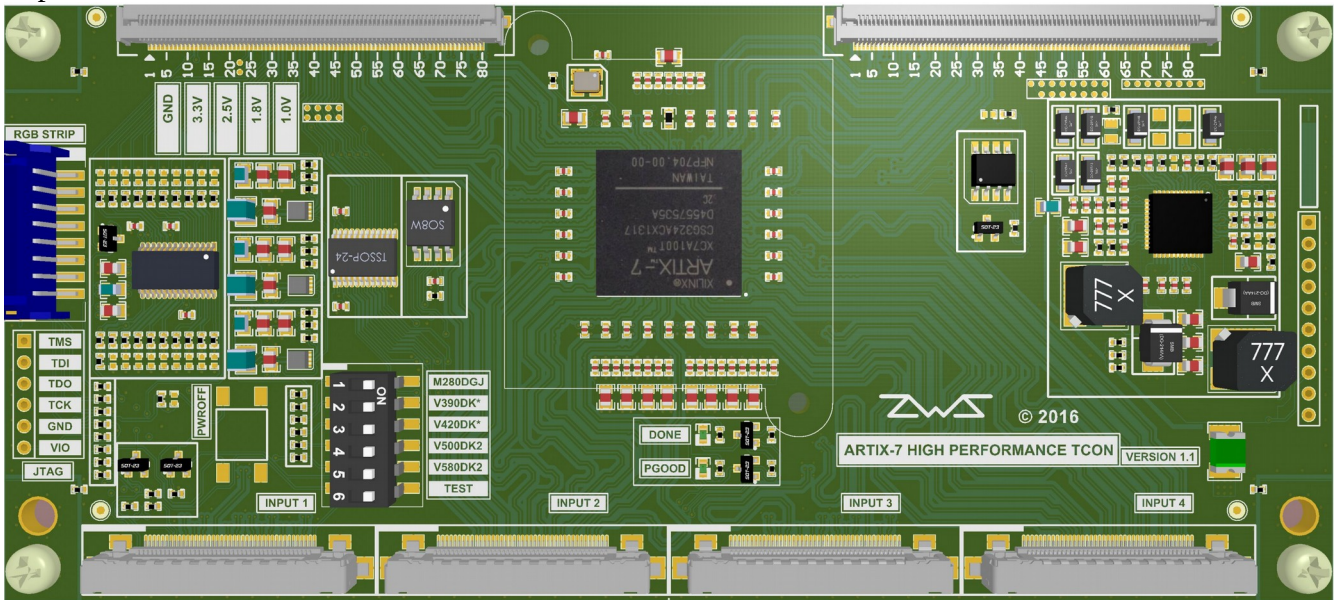
- Two input ports, each with quad-channel LVDS
- Onscreen display shows an autoscaling scrolling realtime graph of framerates
- 3840*2160 @ 120Hz (two input groups)
- 3840*2160 @ 60Hz (one input group)
- 3840*1080 @ 240Hz (two input groups)
- 1920*1080 @ 240Hz (one input group)
- 3840*720 @ 300Hz (two input groups)
- 1280*720 @ 300Hz (one input group)
- 3840*540 @ 480Hz (two input groups)
- 960*540 @ 480Hz (one input group)
- Up to 540MHz Pixel clock per input group
- Up to 276KHz maximum line-rate
- DE-Only video timing simplifies driving requirements
- Active per-bit deskewing of LVDS inputs
- Inter-channel skew of up to 2 pixels is tolerated
- Inter-port skew of up to 3 lines is tolerated
- Dynamic PLL reconfiguration for a wide range of video input frequencies
- 10 bit input (temporal dithering + 8bit panel)
- 10~14V Input voltage
- High-quality power supplies with all-ceramic capacitor design
- Firmware controlled power supplies enable support of multiple panels of varying types.
- Six layer controlled impedance PCB for highest signal integrity
- Output video synchronization signal for use with ZWS backlight drivers
- JTAG connection for firmware update
- Additional connection for dynamic rear-illuminating RGB LED strips (SK6812 type) **(NOT IMPLEMENTED YET)**

PANEL COMPATIBILITY

	PANEL COMPATIBILITY	
M238DCJ-E50	23.8" 9.5ms AAS	WILL NOT WORK
M280DGJ-L30	28" 1ms TN	FULLY SUPPORTED
V390DK1-LS1	39" 6.5ms MVA	FULLY SUPPORTED
M315DJJ-K30	31.5" 9.5ms MVA	WILL NOT WORK
V420DK*	42" 9.5ms MVA	UNTESTED
V500DK2	50" 6.5ms MVA	UNTESTED
V580DK2	58" 6.5ms MVA	UNTESTED

BOARD OVERVIEW

Top view:



There are four 41pin FI-RE41HS connectors, labeled INPUT 1~4. Additionally, there is an 8pin PH2.0 connector on the left edge of the board, labeled “RGB STRIP”. This connection is intended for use with the optional rear illumination package. A labeled JTAG interface on the left edge enables firmware updates.

CONNECTOR PINOUTS

PCB VERSION 1.1	
RGB STRIP	
FI-RE41HS PIN	SIGNAL NAME
1	POWER INPUT
2	POWER INPUT
3	2.5V
4	ENABLE
5	FRAME_SYNC
6	SERIAL_OUTPUT
7	GROUND
8	GROUND

PCB VERSION 1.1	
INPUT 1	
FI-RE41HS PIN	SIGNAL NAME
1	POWER INPUT
2	POWER INPUT
3	POWER INPUT
4	POWER GROUND
5	POWER GROUND
6	POWER GROUND
7	FRAME_SYNC
8	SERIAL_OUTPUT
9	GROUND
10	LVDS EVEN A-
11	LVDS EVEN A+
12	LVDS EVEN B-
13	LVDS EVEN B+
14	LVDS EVEN C-
15	LVDS EVEN C+
16	GROUND
17	LVDS EVEN CLOCK-
18	LVDS EVEN CLOCK+
19	GROUND
20	LVDS EVEN D-
21	LVDS EVEN D+
22	LVDS EVEN E-
23	LVDS EVEN E+
24	SERIAL_INPUT
25	GROUND
26	LVDS ODD A-
27	LVDS ODD A+
28	LVDS ODD B-
29	LVDS ODD B+
30	LVDS ODD C-
31	LVDS ODD C+
32	GROUND
33	LVDS ODD CLOCK-
34	LVDS ODD CLOCK+
35	GROUND
36	LVDS ODD D-
37	LVDS ODD D+
38	LVDS ODD E-
39	LVDS ODD E+
40	GROUND
41	SHUTDOWN

PCB VERSION 1.1	
INPUT 2~4	
FI-RE41HS PIN	SIGNAL NAME
1	POWER INPUT
2	POWER INPUT
3	POWER INPUT
4	POWER GROUND
5	POWER GROUND
6	POWER GROUND
7	FRAME_SYNC
8	NO-CONNECT
9	GROUND
10	LVDS EVEN A-
11	LVDS EVEN A+
12	LVDS EVEN B-
13	LVDS EVEN B+
14	LVDS EVEN C-
15	LVDS EVEN C+
16	GROUND
17	LVDS EVEN CLOCK-
18	LVDS EVEN CLOCK+
19	GROUND
20	LVDS EVEN D-
21	LVDS EVEN D+
22	LVDS EVEN E-
23	LVDS EVEN E+
24	NO-CONNECT
25	GROUND
26	LVDS ODD A-
27	LVDS ODD A+
28	LVDS ODD B-
29	LVDS ODD B+
30	LVDS ODD C-
31	LVDS ODD C+
32	GROUND
33	LVDS ODD CLOCK-
34	LVDS ODD CLOCK+
35	GROUND
36	LVDS ODD D-
37	LVDS ODD D+
38	LVDS ODD E-
39	LVDS ODD E+
40	GROUND
41	NO-CONNECT

PIN DESCRIPTIONS

POWER INPUT	POWER IN	10~14V DC	SYSTEM INPUT POWER	Notes
POWER GROUND	PASSIVE	GROUND		
GROUND	PASSIVE	GROUND		
2.5V	POWER OUT	2.5V DC	I/O VOLTAGE FOR THE FPGA	1
ENABLE	OUTPUT	2.5V LOGIC	HIGH WHEN THE PANEL IS TURNED ON	2
FRAME_SYNC	OUTPUT	2.5V LOGIC	LOW DURING VBLANKING, HIGH OTHERWISE	2
SERIAL_OUTPUT	OUTPUT	2.5V LOGIC	CONTROL SIGNAL FOR SK6812 RGB LED STRIP	2
SERIAL_INPUT	INPUT	HV LOGIC	SERIAL CONTROL INPUT	3, 4
SHUTDOWN	INPUT	HV LOGIC	DISABLES THE DC/DC REGULATORS IF > 2V.	3, 4
LVDS *	INPUT	LVDS	INPUT VIDEO SIGNALS	5

Notes:

- 1) This line is connected to the 2.5V power rail through a 10ohm resistor.
- 2) This line is connected to an FPGA I/O through a 1K ohm resistor. Be careful when using this pin.
- 3) This line is connected to a level shifter. Maximum input voltage is 16V, $V_{IHmin}=2v$, $V_{ILmax}=0.5v$.
- 4) If unused, this signal may be left open. There is a pulldown resistor on the board.
- 5) The LVDS video format is a combination physical electrical level specifications and an overlying bit/pixel/line/frame specification.

LVDS electrical specifications are summarized in the table below. Consult the Artix7 documentation for additional details.

INPUT	COMMON MODE	MIN	0.3V
		MAX	1.425V
DIFFERENTIAL SWING		TYPICAL	1.2V
		MIN	0.1V
		MAX	-
		TYPICAL	-

REAR FACING RGB LEDS (NOT IMPLEMENTED YET)

The FPGA analyzes the near-edge pixels being sent to the panel and sends an appropriate data stream for SK6812 type RGB-LED strips. When attached to the back of the LCD panel and allowed to diffusely reflect off of a wall behind the panel, this ambient lighting appears to extend the screen beyond the bezel. An optional kit includes the required driver board and LED strips.

SERIAL CONTROL INPUT

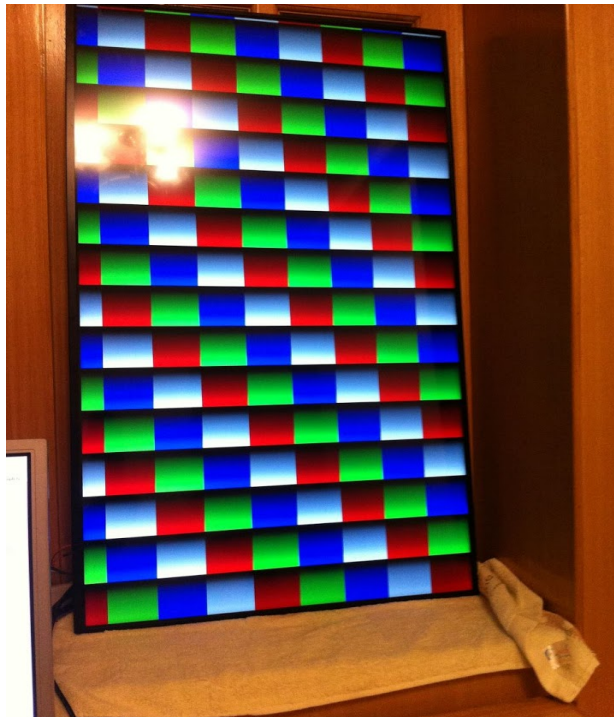
The SERIAL_INPUT signal is used to set some system flags using a single-byte control scheme. With the serial interface operating at 115200 baud, 8n1 configuration. The default values correspond to the all-zeroes case.

BIT POSITION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FIELD NAME	FIRMWARE UPDATE ENABLE	RGB LED STRINGS DISABLE	TARGET CROSSHAIR ENABLE	ON SCREEN DISPLAY ENABLE	DEBUG MODE ENABLE	VESA / JEIDA MODE SELECT	8BIT/10BIT MODE SELECT	CHECKSUM
DEFAULT	OFF	ON	OFF	OFF	OFF	VESA	10BIT	-

If the serial input is held high for more than five seconds without receiving additional bytes, the system will enter debug mode. If the input is held low or left floating, the system will continue operating with the previously set values, or if none were set, the default configuration. This aspect of system configuration is volatile, not being saved through power cycles.

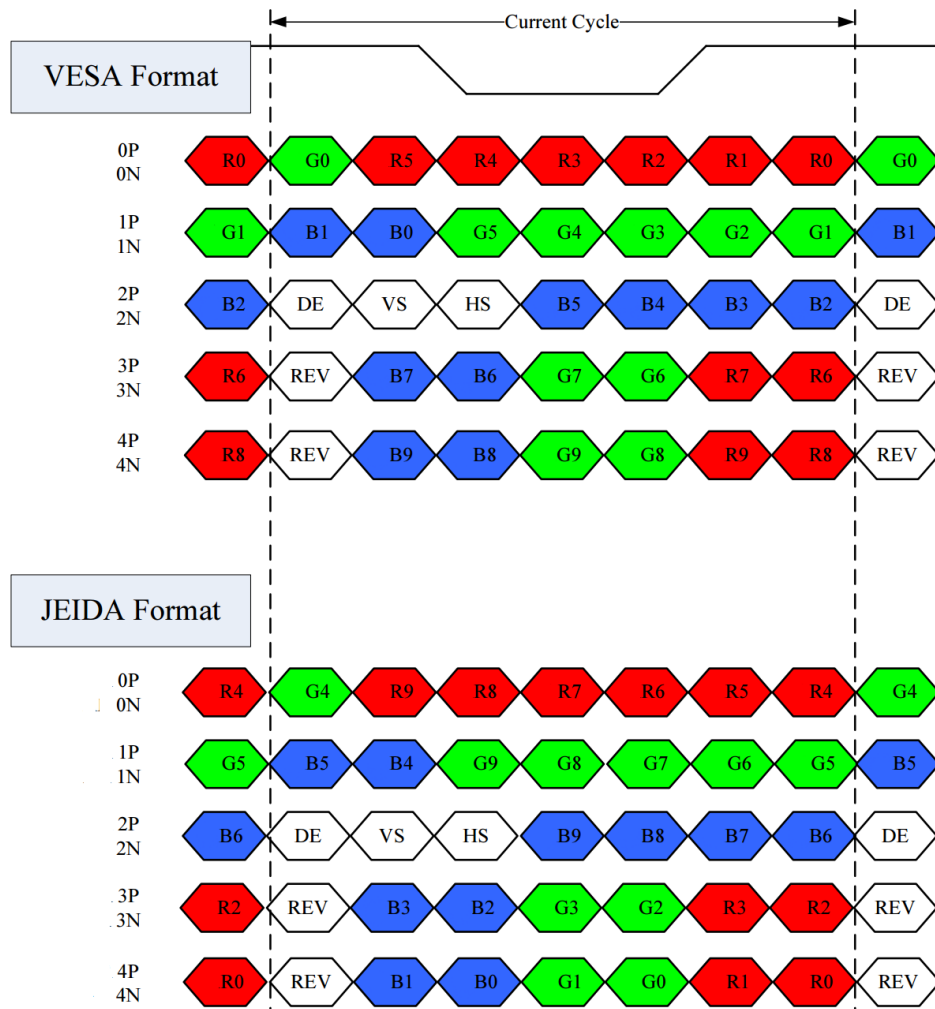
DEBUG MODE

When in debug mode, the system is turned on using an internal test pattern generator. Video inputs are ignored. The test pattern generator cycles through the four supported resolutions, resulting in an image like this one:



TODO: use a better image here

LVDS BIT MAPPING



The mapping of bits onto the LVDS signal lanes is shown here for both VESA and JEIDA modes. For the color channels, bit 9 is the MSB and bit 0 is the LSB. REV signals are reserved and are ignored by the system. DE, VSY, and HSY are the standard data-enable, vertical-sync, and horizontal-sync signals.

LVDS PIXEL MAPPING

There are four input connectors, labeled INPUT1, INPUT2, INPUT3, and INPUT4, with each input connector containing two LVDS channels. These eight channels can be called E1, O1, E2, O2, E3, O3, E4, and O4. Within each group, four channels are interleaved to form the incoming pixel stream. Beginning with pixel 0 in the upper left, E1 carries pixels 0, 4, 8, 12..., E2 carries 1, 5, 9, 13..., O1 carries 2, 6, 10, 14..., and O2 carries 3, 7, 11, 15... TODO: verify if correct ordering

INPUT BEHAVIOR

Inputs E1, O1, E2, and O2 belong to the primary group, and inputs E3, O3, E4, and O4 belong to the secondary group. All clocks within a group must be matched in frequency, but may be offset in phase. If two groups are simultaneously active, the primary group will be displayed on the left hand side of the screen with the secondary on the right. If only one group is active, it will occupy the entire screen. If two groups are used simultaneously, it is absolutely critical that the input streams be vertically synchronized within +/- 3 lines of each other.

Integer scaling of 1:1, 1:2, 1:3, and 1:4 is supported. Only exact 1:1, 1:2, 1:3, and 1:4 mappings are allowed vertically. Video streams which are not exactly 2160, 1080, 720, or 540 lines tall will be replaced with a test pattern and warning. Video streams with excessive width will be displayed with a warning. Nonexact horizontal scaling will result in a horizontally centered image with unused display area blacked-out.

Horizontal and vertical scaling are independent of each other, so non-square pixels are allowed. This situation can be useful, for example, in a 3840*1080@240Hz scenario, if the host system is made aware of the pixel aspect ratio.

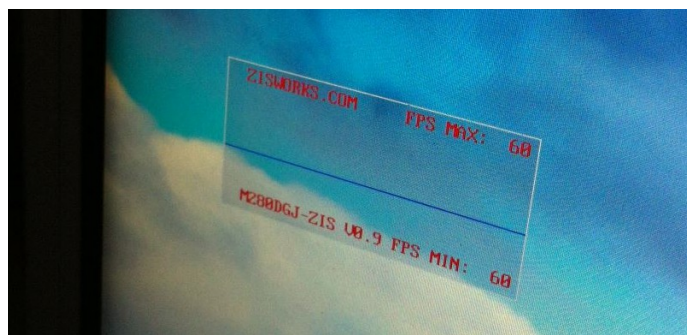
If the input is detected as invalid or partially invalid, a test pattern or overlaid warning will be shown on the screen to alert the user to the problem.

DE-Only timing mode is supported, with the HSYNC and VSYNC signals ignored internally. Any duration of DE being low for more than 8 clocks is considered the end of the current line, and any duration of DE staying low for more than 510 clocks is considered the end of the current frame. There is no set limit for the maximum vertical blanking duration. The system does not require a consistent blanking interval, variable blanking intervals are accepted.

ON SCREEN DISPLAY

An on-screen-display shows the selected panel, firmware version, and a realtime autoscaling scrolling graph of the framerate of the most recent 253 frames, with minimum and maximum values shown. The OSD is alpha-blended with the video stream and overlaid in the upper left corner of the display.

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FIRMWARE UPDATE (JTAG)

Please check zisworks.com/downloads for full firmware update instructions via the JTAG interface.

FIRMWARE UPDATE (SOFTWARE) (NOT IMPLEMENTED YET)

First, switch to single-input 4k60 mode. Then enable the firmware update flag via the serial command interface, then open the firmware update image at 100% zoom level and wait. During and after this process, a message will appear on the screen indicating the status of the update process.

When the firmware update flag has been set, the system will scan the input video stream for special sequences of bits and write them to the system flash. Once integrity of the entire image has been verified, the data will be copied from the temporary flash location into the active boot region of the flash. It is extremely important that the system is not interrupted during this time.